Outline

• SR Latch
• D Latch
• Edge-Triggered D Flip-Flop (FF)
• S-R Flip-Flop (FF)
• J-K Flip-Flop (FF)
• T Flip-Flop (FF)
• Flip-Flops (FFs) with Additional Inputs
• Combinational circuits
  – Outputs depend on present inputs
• Sequential circuits
  – Outputs depend on both present and the past sequence of inputs.
  – Have memory.
SR Latch (2/17)

Combinational Circuit

Input

Output

Sequential Circuit

Input Set 1

Output Set 1

Input Set 2

Output Set 2
The circuit can assume an initial and stable state: SR/PQ=00/10.
SR Latch (4/17)

- SR/PQ=10/01 is also stable.

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>NOR</th>
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<tbody>
<tr>
<td>0</td>
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SR Latch (5/17)

- SR/PQ=00/01 is also stable.

<table>
<thead>
<tr>
<th>X</th>
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</table>
SR Latch (6/17)

- SR/PQ=01/10 is also stable.
- SR/PQ=00/10 is also stable.

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>NOR</th>
</tr>
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<tr>
<td>0</td>
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<td>1</td>
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<td>0</td>
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</tbody>
</table>
SR Latch (7/17)

X  Y  NOR
0  0  1
0  1  0
1  0  0
1  1  0
SR Latch (8/17)

X   Y   NOR
0   0   1
0   1   0
1   0   0
1   1   0
SR Latch (9/17)

The change between any two of 00, 10, 01 will reach a stable state.
What is PQ when the circuit is stable?

<table>
<thead>
<tr>
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<th>Y</th>
<th>NOR</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
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</tbody>
</table>

The NOR function values for the given input combinations.
SR Latch (11/17)

• SR=11 is restricted in SR latch.
• PQ cannot be both 1.
SR Latch (12/17)

• When SR=10, PQ=01 is stable.
• When SR=01, PQ=10 is stable.
• When SR=00, both PQ=10 and PQ=01 are stable.
• Note
  – In the stable states, P=Q’
  – Any change to SR=00 will not change PQ.
  – SR=00 is used to keep states (remember what happened.)
SR Latch (13/17)

S: Set Q
R: Reset Q
SR Latch (14/17)

• How to draw a truth table for an SR latch?
  – Input?
  – Output?
SR Latch (15/17)

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<thead>
<tr>
<th></th>
<th>0</th>
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<td>1</td>
<td>1</td>
<td></td>
<td></td>
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<tr>
<td>0 1</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
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<tr>
<td>1 0</td>
<td>0</td>
<td>1</td>
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<tr>
<td>1 1</td>
<td>1</td>
<td>1</td>
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</tbody>
</table>

\[ Q(t + \epsilon) = S(t) + R'(t) Q(t) \]
SR Latch (16/17)

- Alternatively, an SR latch can be realized using NAND gates.
SR Latch (17/17)

- Alternatively, an SR latch can be realized using NAND gates.

<table>
<thead>
<tr>
<th>S-bar</th>
<th>R-bar</th>
<th>Q</th>
<th>Q^+</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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<td>0</td>
<td>0</td>
</tr>
<tr>
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<td>0</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>
Gated D Latch (1/3)

- What are S and R when G=0?
- G=0 keeps states: \( Q^+ = D \).
- Can SR=11 ever occur?
- \( Q^+ = D \) when G=1.
Gated D Latch (2/3)

\[
\begin{array}{c|c|c|c|c}
GD & 00 & 01 & 11 & 10 \\
\hline
Q & 0 & 0 & 1 & 0 \\
\hline
0 & 0 & 0 & 1 & 0 \\
1 & 1 & 1 & 1 & 0 \\
\end{array}
\]

\[Q^+ = G'Q + GD\]

- No “do not care” terms.
Gated D Latch (3/3)

- if(G==1){
  - \( Q^+ = D \);
- }else{
  - \( Q^+ = Q \);
- }

Edge-Triggered D Flip-Flop (FF)

1/3

- If the G signal in the D latch is connected to a clock input, the output changes only in response to the clock, not to a change in D.
- And we call this latch a D Flip-Flop (FF).

\[ Q^+ = D \]

(a) Rising-edge trigger

(b) Falling-edge trigger
Edge-Triggered D Flip-Flop (FF) (2/3)

(a) Construction from two gated D latches

(b) Time analysis
Edge-Triggered D Flip-Flop (FF) (3/3)

Note Q does not change during Ck=0.

• Timing for D Flip-Flops (FF) (Falling-Edge Trigger)
S-R Flip-Flop (FF) (1/3)

- $Q^+$ changes in response to the clock signal.
S-R Flip-Flop (FF) (2/3)

- When \( \text{CLK}=0 \)
  - \( P^+ = S_1 + R_1'P \)
- When \( \text{CLK}=1 \)
  - \( Q^+ = P \)

(a) Implementation with two latches

(b) Timing analysis
S-R Flip-Flop (FF) (3/3)

• Why master-slave Flip-Flops (FFs)?
  – The master Flip-Flop (FF) holds the output for in the first half clock cycle.
  – When the slave Flip-Flop (FF) updates and outputs, the master is closed.
  – This mechanism guarantees that the final output changes only once in a clock cycle.
JK Flip-Flop (FF) (1/2)

• An extended version of the SR Flip-Flop (FF)
  – J corresponds to S
  – K corresponds to R

• J  K  Q  Q^+

• 0  0  0  0
• 0  0  1  1
• 0  1  0  0
• 0  1  1  0
• 1  0  0  1
• 1  0  1  1
• 1  1  0  1
• 1  1  1  0

JK can be 11. This configuration changes the state of Q.
JK Flip-Flop (FF) (2/2)

- $S_1 = J \cdot Q' \cdot \text{CLK}'$
- $R_1 = K \cdot Q \cdot \text{CLK}'$
- $S_1$ and $R_1$ cannot be 1 at the same time.
T Flip-Flop (FF) (1/2)

- $T=0 \rightarrow$ no state change
- $T=1 \rightarrow$ state changes

$Q^+ = T \oplus Q$

\[
\begin{array}{ccc}
T & Q & Q^+ \\
0 & 0 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]
T Flip-Flop (FF) (2/2)

(a) Conversion of J-K to $T$

(b) Conversion of $D$ to $T$
Summary (1/8)

• All the Flip-Flops (FFs) and D latch are based on SR latch.

• SR latch can be described using
  – $Q^+=S+R'Q$
  – $S=1$ sets $Q$
  – $R=1$ resets $Q$
  – SR=00 keeps states (Q does not change.)
Summary (2/8) $Q^+ = S + R'Q$

- Gated D latch
  - $S = DG$
  - $R = D'G$
  - When $G=0$, $SR==00 \implies$ state kept.
  - When $G=1$, $Q=D$
    - When $D=0$, $SR=01 \implies$ reset $Q \implies Q=0$
    - When $D=1$, $SR=10 \implies$ set $Q \implies Q=1$
Summary (3/8) $Q^+ = S + R'Q$

- When $G$ is a clock signal, two gated D latches comprise an edge-triggered D Flip-Flop (FF).

- Note $Q$'s waveform is not exactly the same with D's.
Summary (4/8) $Q^+ = S + R'Q$

- SR Flip-Flop (FF)
  - Master and slave
  - When the master receives the input and updates, the slave is close.
  - When the slave outputs, the master does not respond to any input change.
Summary (5/8) $Q^+ = S + R’Q$

- SR Flip-Flop (FF) (cont)
  - When CLK is low,
    - $S_1R_1 = SR \Rightarrow P^+ = S + R’P$, master is updated
    - $S_2R_2 = 00 \Rightarrow Q$ does not change
Summary (6/8) \( Q^+ = S + R'Q \)

- SR Flip-Flop (FF) (cont)
  - When CLK is high,
    - \( S_R_1 = 00 \) \( \Rightarrow \) \( P \) does not change
    - master does not respond to inputs
    - \( S_2 R_2 = PP' \) \( \Rightarrow \) \( Q^+ = P + (P')'Q = P \)
Summary (7/8) $Q^+ = S + R'Q$

- SR Flip-Flop (FF) (cont)

<table>
<thead>
<tr>
<th>SR</th>
<th>10</th>
<th>01</th>
<th>10</th>
<th>01</th>
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<tbody>
<tr>
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<td></td>
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</tr>
<tr>
<td>CLK</td>
<td>low</td>
<td>high</td>
<td>low</td>
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<tr>
<td>Q</td>
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- The final output, Q, was not affected by $01$.  
- Master
- Slave
Summary (8/8) $Q^+ = S + R'Q$

- **JK Flip-Flop (FF)**
  - Very similar to SR master-slave Flip-Flop (FF)
  - Except JK=11 inverts the output

- **T Flip-Flop (FF)**
  - $T=1 \implies$ inverts the output
  - $T=0 \implies$ keeps the same output
Flip-Flops (FFs) with Additional Inputs (1/3)

• Clear and Preset signals are two asynchronous signals and do not depend on CLK.
Flip-Flops (FFs) with Additional Inputs (2/3)

<table>
<thead>
<tr>
<th></th>
<th>CLK</th>
<th>D</th>
<th>ClrN</th>
<th>PreN</th>
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Flip-Flops (FFs) with Additional Inputs (3/3)

- Clock enable signal

(a) Gating the clock
(b) D-CE symbol
(c) Implementation